What is claimed is:

1. A method of verifying a mask for a mask ROM, comprising the steps of:

selecting a first and second chips manufactured by a process with said mask;

implanting a random code into said first chip and testing said first chip for generating a first test result;

implanting a reverse tone code derived from said random code into said second chip and testing said second chip for generating a second test result; and

comparing said first and second test results for determining if said mask is defective.

2. A method according to claim 1, wherein said first and second chips are selected from two wafers, respectively.

3. A method according to claim 1, wherein said first and second chips are selected from two die regions on a wafer.

4. A method of verifying a mask for a mask ROM,

comprising the steps of:

selecting a plurality of chips manufactured by a process with said mask;

implanting a plurality of codes exclusive to each other into said plurality of chips, respectively;

testing said plurality of chips for generating a plurality of test results; and

comparing said plurality of test results for determining if said mask is defective.

5. A method according to claim 4, wherein said plurality of chips are selected from individual wafers, respectively.

6. A method according to claim 4, wherein said plurality of chips are selected from individual die regions on a wafer.